WHAT IS CLAIMED IS:

1. A sequencing method for accessing shared system resources capable of determining the priority of transactions initiated by a plurality of master controllers, comprising the steps of:

providing each transaction with a transaction identification value to determine an order of execution of each transaction;

providing each transaction with a master identification value to label the initiating master controller of each transaction; and

gathering transactions having an identical master identification value and accessing the shared system resource in sequence according to the transaction identification value.

2. The method of claim 1, wherein the transactions include write transactions and read transactions.

3. The method of claim 2, wherein the step of providing each transaction with the transaction identification value includes the sub-steps of:

providing the first transaction with the transaction identification value of 0;

adding 1 to the transaction identification value when the previous transaction of the read transaction is the read transaction;

adding 0 to the transaction identification value when the previous transaction of the read transaction is the write transaction;

adding 1 to the transaction identification value when the previous transaction of the write transaction is the read transaction;

adding 0 to the transaction identification value when the previous transaction of the write transaction is the write transaction.

4. The method of claim 3, wherein the step of accessing the shared system resource according to the transaction identification value includes the sub-steps of:

picking up the transaction having the smallest transaction identification value and executing the transaction to access the shared system resource; and

executing the write transactions to access the shared system resource before the read transactions if two or more transactions have the same smallest transaction identification value.

5. The method of claim 1, wherein the sequencing method also incorporates a flush and a fence signal provided by an accelerated graphic port (AGP) bus to ensure proper transaction execution sequence.

6. A bridging system for accessing a shared system resource, comprising:

at least one master controller, wherein the at least one master controller is capable of submitting a plurality of write transactions and a plurality of read transactions;

a first bus coupled to the at least one master controller;

a bridging device coupled to the first bus for transporting the read transactions and the write transactions;

a second bus coupled to the bridging device; and

a chipset coupled to the second bus and the shared system resource for selecting one of the read transactions or the write transactions initiated from one of the at least one master controller so that the shared system resource is accessed.

7. The bridging system of claim 6, wherein the first bus is a PCI bus.

8. The bridging system of claim 6, wherein the second bus is an accelerated graphic port (AGP) bus.

9. The bridging system of claim 6, wherein each read transaction or each write transaction has a transaction identification value for determining execution sequence.

10. The bridging system of claim 9, wherein each read transaction or each write transaction has a master identification value for identifying the initiating master controller.

11. The bridging system of claim 9, wherein the chipset further includes:

a read queue for holding the master identification values and the transaction identification values of all read transactions;

a write queue for holding the master identification values and the transaction identification values of all write transactions;

a plurality of master controller read queues, wherein each master controller read queue holds all the read transaction identification values having identical master identification value; and

a plurality of master controller write queues, wherein each master controller read queue holds all the write transaction identification values having identical master identification value.